SSR811/SSR812

Technical Data
Data Sheet N1594 Rev. -

Reset Circuits with Manual Reset Input

Description:

SSR811/SSR812 are low-power microprocessor (µP) supervisory circuits used to monitor power supplies in µP and digital systems. They provide applications with benefits of circuit reliability and low cost by eliminating external components. SSR811/SSR812 also offer a manual reset input.
These devices perform as valid singles in applications with Vcc ranging from 6.0V down to 0.9V. The reset signal lasts for a minimum period of 140ms whenever VCC supply voltage falls below preset threshold. Both SSR811 and SSR812 were designed with a reset comparator to help identify invalid signals, which last less than 140ms. The only difference between them is that they have an active-low $\overline{\text{RESET}}$ output and active-high RESET output, respectively.
Low supply current (1µA) makes SSR811/SSR812 ideal for portable equipment. The devices are available in SOT-23-5 package.

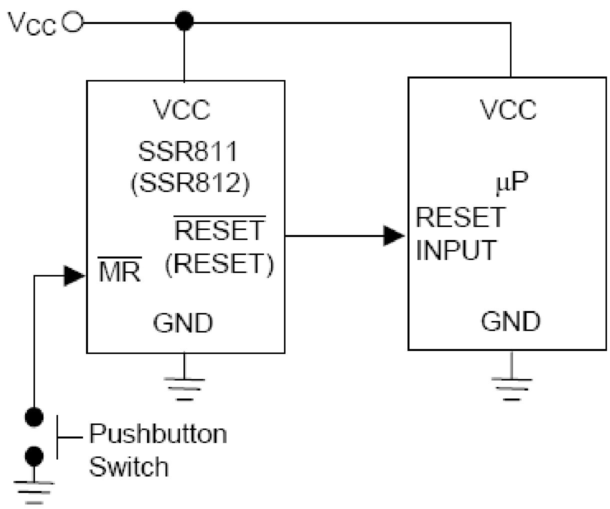
Features:

- **Ultra Low Supply Current 1µA(typ.)**
- **Guaranteed Reset Valid to Vcc=0.9V**
- **Available in two Output Types: Push-Pull Active Low (SSR811), Push-Pull Active High (SSR812)**
- **140ms Min. Power-On Reset Pulse Width**
- **Internally Fixed Threshold 2.3V, 2.6V, 2.7V, 2.9V, 3.1V, 4.0V, 4.4V, and 4.6V**
- **Tight Voltage Threshold Tolerance: 1.5%**
- **Low Profile Package: SOT-23-5.**

Applications:

- **Notebook Computers**
- **Digital Still Cameras**
- **PDAs**
- **Critical Microprocessor Monitoring**

Typical application circuit:



Ordering Information:

SSR811 -XXXXX
SSR812 -XXXXX

PACKING TYPE
TB: TUBE
TR: TAPING & REEL

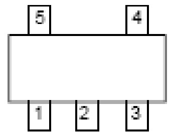
PACKAGING TYPE
D: SOT-23-5

RESET THRESHOLD VOLTAGE
- 23: 2.3V
- 26: 2.6V
- 27: 2.7V
- 29: 2.9V
- 31: 3.1V
- 40: 4.0V
- 44: 4.4V
- 46: 4.6V

PIN CONFIGURATION

SOT-23-5

TOP VIEW
1: GND
2: NC
3: $\overline{\text{RESET}}$ (RESET)
4: $\overline{\text{MR}}$
5: VCC



Marking Diagram:

Part No.	Marking
SSR811-26DTR	**BQ26G**
SSR811-29DTR	**BQ29G**
SSR811-31DTR	**BQ31G**
SSR811-44DTR	**BQ44G**
SSR811-46DTR	**BQ46G**
SSR812-23DTR	**BR23G**
SSR812-26DTR	**BR26G**
SSR812-29DTR	**BR29G**
SSR812-31DTR	**BR31G**
SSR812-40DTR	**BR40G**
SSR812-44DTR	**BR44G**
SSR812-46DTR	**BR46G**

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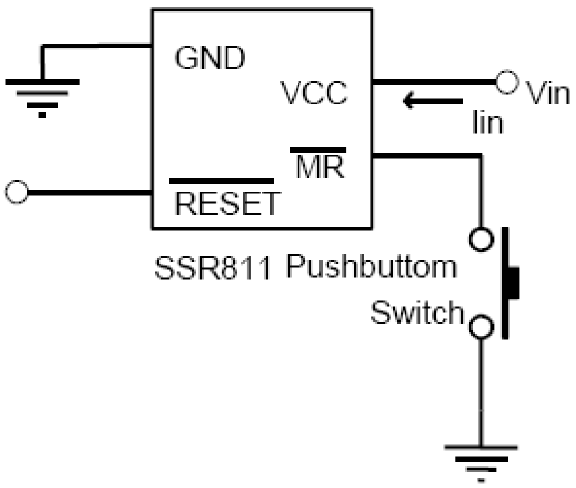
Absolute Maximum Ratings:

- V_{CC} ....-0.3V~6.5V
- RESET, $\overline{RESET}$..-0.3V ~ (VCC+0.3V)
- Input Current (V_{CC}, $\overline{MR}$).. 20mA
- Output Current (RESET or $\overline{RESET}$)..20mA
- Continuous Power Dissipation (T_A = +70°C) 320mW
- Operating Junction Temperature Range .... –40°C to 85°C
- Junction Temperature ....125°C
- Storage Temperature Range ....–65°C ~ 150°C
- Lead Temperature (Soldering) 10 sec. ....260°C

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Test Circuit



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Electrical Characteristics (Typical values are at T_A=25°C, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V_{CC}			0.9		6	V
Supply Current	I_{CC}	$V_{CC} = V_{TH}$ +0.1V			1	3	μA
Reset Threshold	V_{TH}	SSR811-23	T_A=+25°C	2.265	2.3	2.335	V
			T_A= -40°C to +85°C	2.254		2.346	
		SSR811-26	T_A=+25°C	2.561	2.6	2.639	
			T_A= -40°C to +85°C	2.548		2.652	
		SSR811-27	T_A=+25°C	2.660	2.7	2.741	
			T_A= -40°C to +85°C	2.646		2.754	
		SSR811-29	T_A=+25°C	2.857	2.9	2.944	
			T_A= -40°C to +85°C	2.842		2.958	
		SSR811-31	T_A=+25°C	3.054	3.1	3.147	
			T_A= -40°C to +85°C	3.038		3.162	
		SSR811-40	T_A=+25°C	3.940	4.0	4.060	
			T_A= -40°C to +85°C	3.920		4.080	
		SSR811-44	T_A=+25°C	4.334	4.4	4.466	
			T_A=-40°C to +85°C	4.312		4.488	
		SSR811-46	T_A=+25°C	4.531	4.6	4.669	
			T_A=-40°C to +85°C	4.508		4.692	
V_{CC} to Reset Delay	T_{RD}	$V_{CC}=V_{TH}$ to (V_{TH} –0.1V), V_{TH}=3.1V			20		μS
Reset Active Timeout Period	T_{RP}	$V_{CC} = V_{TH(MAX)}$	T_A=+25°C	140	230	560	mS
			T_A= -40°C to +85°C	100		1030	
$\overline{MR}$ to Reset Propagation Delay	T_{MD}	Vcc=6V			0.5		μS
$\overline{MR}$ Input Threshold	V_{IH}			0.7V_{CC}			V
	V_{IL}					0.25V_{CC}	
$\overline{MR}$ Pull-Up Resistance				10	20	30	KΩ
$\overline{RESET}$ Output Voltage	V_{OH}	$V_{CC}=V_{TH}$+0.1V, I_{SOURCE}=1mA		0.8V_{CC}			V
	V_{OL}	$V_{CC}=V_{TH}$ - 0.1V, I_{SINK}=1mA				0.2Vcc	
RESET Output Voltage	V_{OH}	$V_{CC}=V_{TH}$+0.1V, I_{SOURCE}=1mA		0.8V_{CC}			V
	V_{OL}	$V_{CC}=V_{TH}$ - 0.1V, I_{SINK}=1mA				0.2Vcc	

Note: 1. Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

2. $\overline{RESET}$ output is for SSR811; RESET output is for SSR812.

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Typical Performance Characteristics

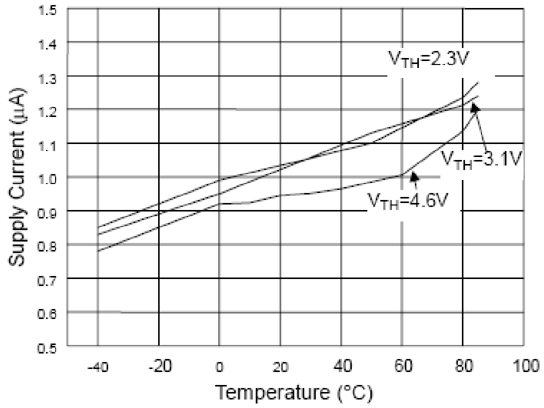


Fig 1 Supply Current vs. Temperature

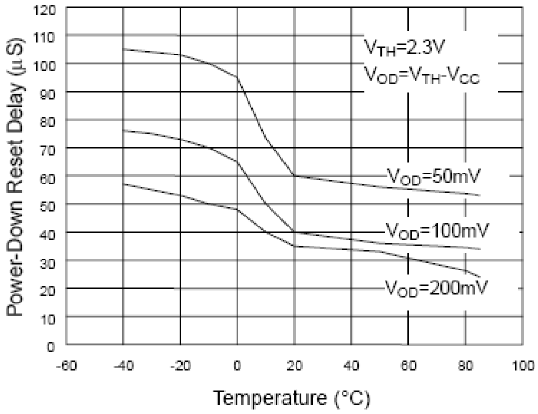


Fig 2 Power-Down Reset Delay vs. Temperature

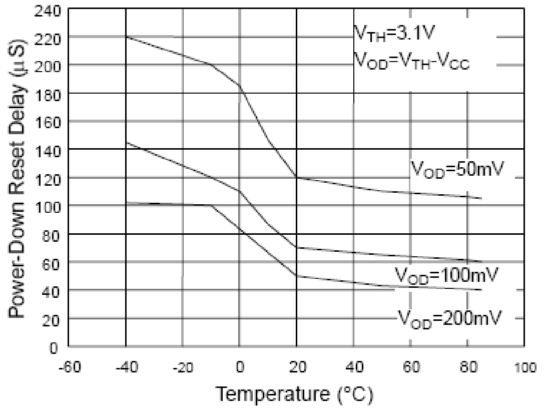


Fig 3 Power-Down Reset Delay vs. Temperature

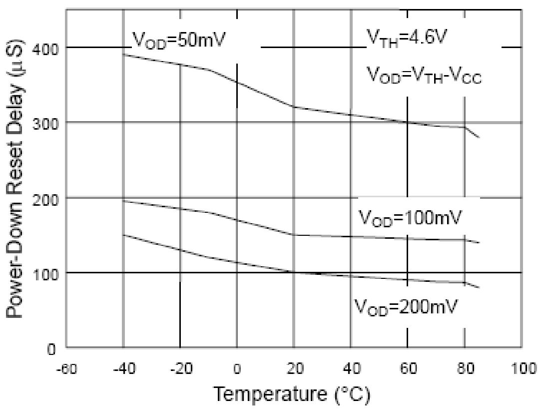


Fig 4 Power-Down Reset Delay vs. Temperature

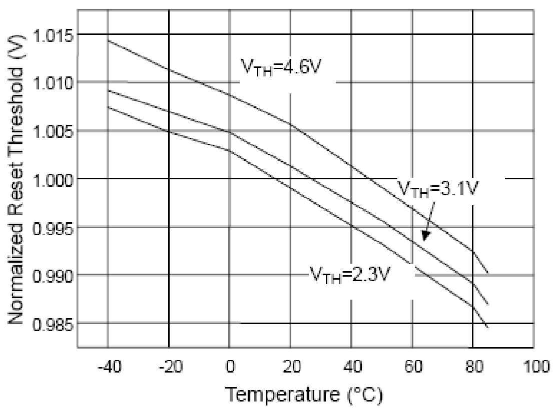


Fig 5 Normalized Reset Threshold vs. Temperature

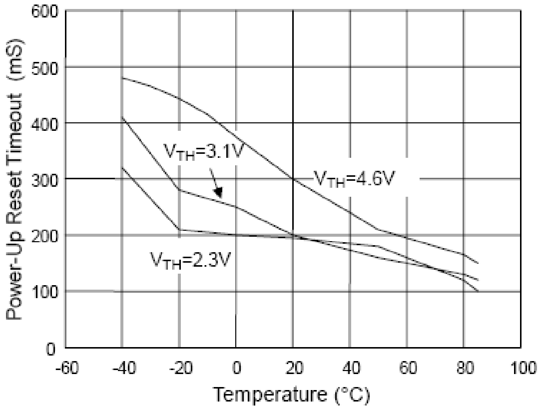
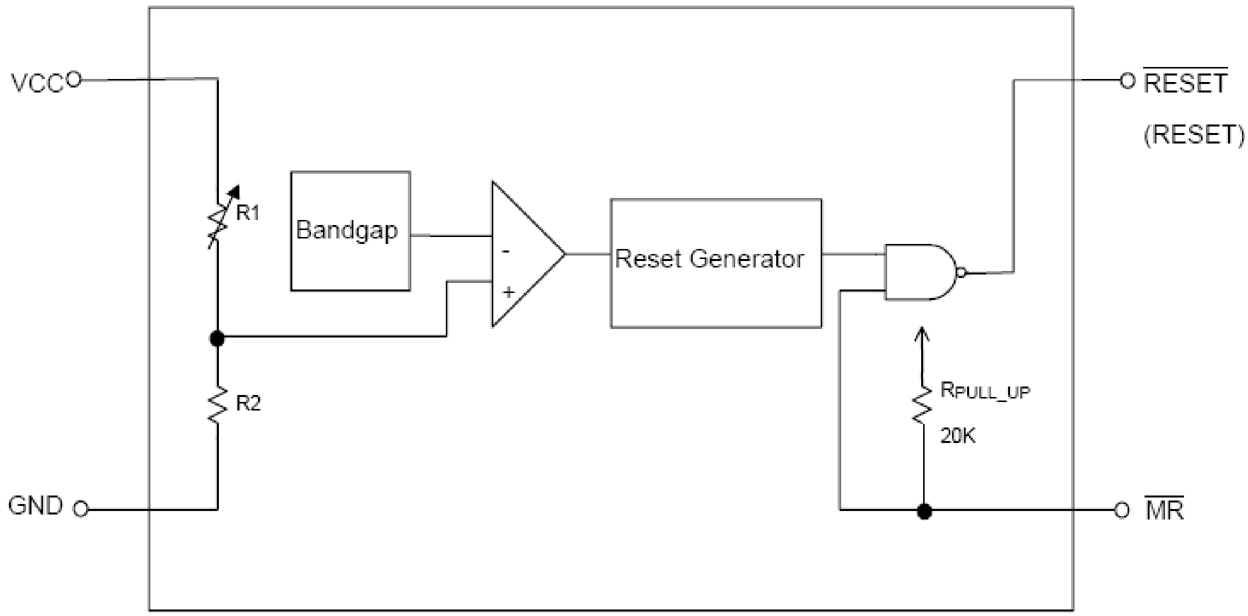


Fig 6 Power-Up Reset Timeout vs. Temperature

Reset Circuits with Manual Reset Input

Block Diagram



Pin Descriptions

GND Pin	: Ground.
$\overline{\text{RESET}}$ Pin (SSR811)	: Active low output pin. $\overline{\text{RESET}}$ Output remains low while Vcc is below the reset threshold.
RESET Pin (SSR812)	: Active high output pin. RESET output remains high while Vcc is below the reset threshold.
$\overline{\text{MR}}$ Pin	: Logic low manual reset input. This active-low input has an internal 20kΩ pull-up resistor. It can be driven by a TTL or CMOS, or shorted to ground with a switch. Leave open when unused.
Vcc Pin	: Supply voltage.

Detail Descriptions of Technical Terms

RESET OUTPUT

µP will be activated at a valid reset state. These µP supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

$\overline{\text{RESET}}$ is guaranteed to be a logic low for V_{TH}>VCC>0.9V. Once VCC exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the reset timeout period; after this interval, $\overline{\text{RESET}}$ goes high.

If a brownout condition occurs (VCC drops below the reset threshold), $\overline{\text{RESET}}$ goes low. Any time VCC goes below the reset threshold, the internal timer resets to zero, and $\overline{\text{RESET}}$ goes low. The internal timer is activated after VCC returns above the reset threshold, and $\overline{\text{RESET}}$ remains low for the reset timeout period.

The manual reset input ($\overline{\text{MR}}$) can also initiate a reset. SSR812 has an active-high RESET output that is the inverse of SSR811's $\overline{\text{RESET}}$ output.

MANUAL RESET INPUT

Many µP-based products require manual reset capability, allowing operators, test technicians, or external logic circuitry to initiate a reset. Logic low on $\overline{\text{MR}}$ asserts reset. Reset will remain asserted for the Reset Active Timeout Period (t_{RP}) after $\overline{\text{MR}}$ returns high. This input has an internal 20KΩ pull-up resistor, so it can be floating if it is not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Another alternative is to connect a normal switch from $\overline{\text{MR}}$ to GND to create a manual reset function. Connecting a 0.1µF capacitor from $\overline{\text{MR}}$ to ground can provide noise immunity to prevent noise caused by long cables of $\overline{\text{MR}}$ or noisy environment.

BENEFITS OF HIGHLY ACCURATE RESET THRESHOLD

SSR811/SSR812 with specified voltage as 5V±10% or 3V±10% are ideal for systems using a 5V±5% or 3V±5% power supply. The reset is guaranteed to assert after the power supply falls out of regulation, but before power drops below the minimum specified operating voltage range of the system ICs. The pre-trimmed thresholds are reducing the range over which an undesirable reset may occur.

Application Information

NEGATIVE-GOING VCC TRANSIENTS
In addition to issuing a reset to the μP during power-up, power-down, and brownout conditions, SSR811 series are relatively resistant to short-duration negative-going VCC transient.

ENSURING A VALID RESET OUTPUT DOWN TO VCC=0
When VCC falls below 0.9V, SSR811 $\overline{\text{RESET}}$ output no longer sinks current; it becomes an open circuit. In this case, high-impedance CMOS logic inputs connecting to $\overline{\text{RESET}}$ can drift to undetermined voltages. Therefore, SSR811/SSR812 with CMOS is perfect for most applications of VCC below 0.9V. However in applications where $\overline{\text{RESET}}$ must be valid down to 0V, adding a pull-down resistor to $\overline{\text{RESET}}$ causes any leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low.

INTERFACING TO μP WITH BIDIRECTIONAL RESET PINS
μPs with bidirectional reset pins can contend with SSR811/812 reset outputs. If SSR811 $\overline{\text{RESET}}$ output is asserted high and the μP wants to pull it low, indeterminate logic levels may occur. To correct such cases, connect a resistor between SSR811 $\overline{\text{RESET}}$ (or SSR812 $\overline{\text{RESET}}$) output and the μP reset I/O. Buffer the reset output to other system components.

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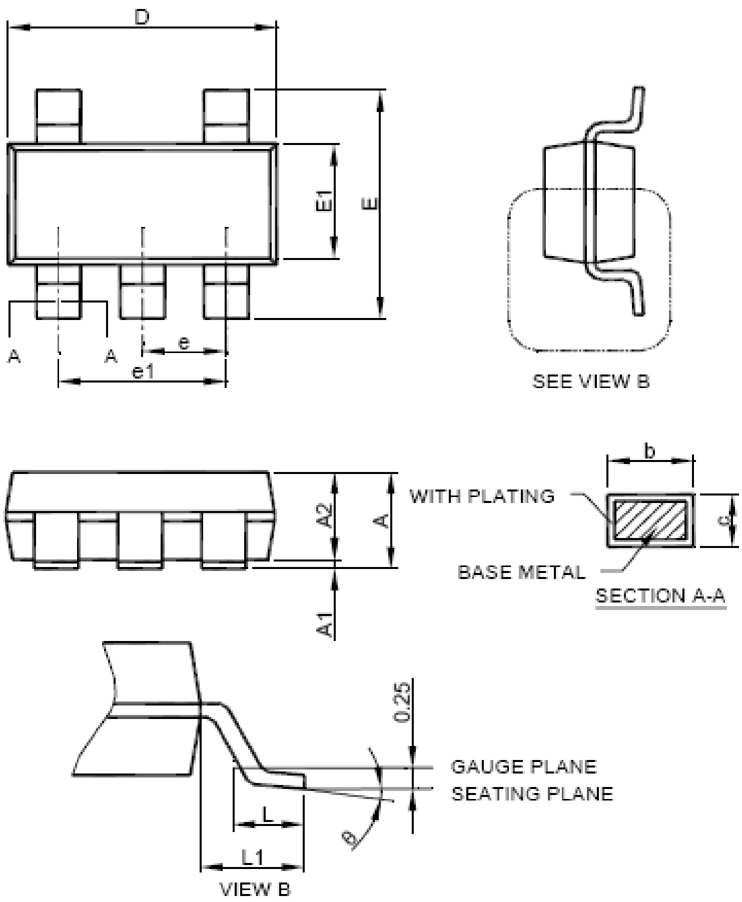
Physical Dimensions

SOT-23-5 (unit: mm)



SYMBOL	SOT-23-5	
	MILLIMETERS	
	MIN.	MAX.
A	0.95	1.45
A1	0.05	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L1	0.60 REF	
q	0°	8°

Note : 1. Refer to JEDEC MO-178AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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